What is claimed is:

1. A floating-gate memory cell, comprising:

a gate stack having a control-gate layer and having a floating-gate layer, wherein the gate stack is overlying an upper well region and wherein the upper well region has a first conductivity type;

a drain region in the upper well region, wherein the drain region has a second conductivity type different from the first conductivity type;

a source region in the upper well region and having the second conductivity type;

a conductive trace coupled to the source region; and

a source-line contact extending from the conductive trace to a lower well region;

wherein the lower well region has the second conductivity type; and

wherein the upper well region is formed in the lower well region.

2. The floating-gate memory cell of claim 1, wherein the conductive trace is formed in the upper well region.

3. The floating-gate memory cell of claim 1, wherein the conductive trace is a conductively-doped region formed in the upper well region and having the second conductivity type.

4. The floating-gate memory cell of claim 1, wherein the conductive trace contains a metal silicide.

5. The floating-gate memory cell of claim 1, wherein the conductive trace is formed on the upper well region.

6. The floating-gate memory cell of claim 1, wherein the source-line contact comprises a columnar trench of conductive fill material.

7. The floating-gate memory cell of claim 1, wherein the source-line contact comprises a conductive fill material formed on sidewalls and a bottom of a contact hole and wherein the sidewalls of the contact hole are defined by the upper well region and the bottom of the contact hole is defined by an exposed portion of the lower well region.

8. The floating-gate memory cell of claim 1, wherein the source-line contact comprises a conductive material and wherein the conductive material includes at least one material selected from the group consisting of an implanted conductively-doped region having the second conductivity type, a diffused conductively-doped region having the second conductivity type, conductively-doped polysilicon having the second conductivity type, a silicide, a polycide, a metal, a metal alloy, and a conductive metal oxide.

9. The floating-gate memory cell of claim 1, wherein the first conductivity type is a p-type conductivity and the second conductivity type is an n-type conductivity.

10. The floating-gate memory cell of claim 1, wherein the source-line contact is laterally displaced from the source region.

11. The floating-gate memory cell of claim 1, wherein the conductive trace is further coupled between at least one additional source region and the source-line contact.

12. A memory device, comprising:

a substrate having a first conductivity type;

a lower well region in the substrate, wherein the lower well region has a second conductivity type different from the first conductivity type;

an upper well region in the lower well region, wherein the upper well region has the first conductivity type;

a plurality of word lines;

a plurality of bit lines; and

a plurality of floating-gate memory cells, wherein each floating-gate memory cell comprises:

a gate stack having a control-gate layer coupled to one of the word lines and having a floating-gate layer interposed between the control-gate layer and the upper well region;

a drain region in the upper well region coupled to one of the plurality of bit lines, wherein the drain region has the second conductivity type;

a source region in the upper well region and having the second conductivity type;

a conductive trace coupled to the source region; and

a source-line contact extending from the conductive trace to a lower well region.

13. The memory device of claim 12, wherein each source-line contact is laterally displaced from each source region and wherein each source-line contact is coupled to at least one source region.

14. The memory device of claim 12, wherein two or more adjacent source regions are commonly coupled through the conductive trace and the source line contact.

15. A floating-gate memory cell, comprising:

a gate stack having a control-gate layer and having a floating-gate layer, wherein the gate stack is overlying a p-well and wherein the p-well is enclosed in an n-well formed in a p-type semiconductor substrate;

an n^+-type drain region in the p-well;

an n^+-type source region in the p-well;

a source-line contact extending below the n^+-type source region to the n-well; and

a conductive trace in the p-well and coupled between the n^+-type source region and the source-line contact.

16. The floating-gate memory cell of claim 15, wherein the conductive trace is further coupled between at least one additional n^+-type source region and the source-line contact.

17. The floating-gate memory cell of claim 15, wherein the conductive trace is further coupled to at least one additional source-line contact.

18. The floating-gate memory cell of claim 15, wherein the conductive trace contains a conductive material selected from the group consisting of a conductively-doped silicon-containing material and a metal silicide.

19. The floating-gate memory cell of claim 15, wherein the source-line contact is laterally displaced from the source region.

20. A floating-gate memory cell, comprising:

a gate stack having a control-gate layer and having a floating-gate layer, wherein the gate stack is overlying a p-well and wherein the p-well is enclosed in an n-well formed in a p-type semiconductor substrate;

an n^+-type drain region in the p-well;

an n^+-type source region in the p-well;

a source-line contact extending below the n^+-type source region to the n-well; and

an n^+-type conductive trace in the p-well and coupled between the n^+-type source region and the source-line contact.

21. A memory device, comprising:

a p-type semiconductor substrate;

an n-well in the substrate;

a p-well enclosed in the n-well;

a plurality of word lines;

a plurality of bit lines; and

a plurality of floating-gate memory cells, wherein each floating-gate memory cell comprises:

a gate stack having a control-gate layer coupled to one of the word lines and having a floating-gate layer interposed between the control-gate layer and the p-well;

an n^+-type drain region in the p-well coupled to one of the plurality of bit lines;

an n^+-type source region in the p-well;

a source-line contact extending below the n^+-type source region to the n-well; and

a conductive trace in the p-well and coupled between the n^+-type source region and the source-line contact.

22. An electronic system, comprising:

a processor; and

a memory device coupled to the processor, wherein the memory device includes an array of floating-gate memory cells arranged in rows and columns with word lines coupled to rows of floating-gate memory cells and bit lines coupled to columns of floating-gate memory cells, and wherein at least one of the floating-gate memory cells comprises:

a gate stack having a control-gate layer coupled to a word line and having a floating-gate layer interposed between the control-gate layer and an upper well region having a first conductivity type;

a drain region in the upper well region coupled to a bit line, wherein the drain region has a second conductivity type different from the first conductivity type; and

a source region in the upper well region and having the second conductivity type;

a conductive trace coupled to the source region; and

a source-line contact extending from the conductive trace to a lower well region underlying the upper well region, the lower well region having the second conductivity type.

23. An electronic system, comprising:

a processor; and

a memory device coupled to the processor, wherein the memory device includes an array of floating-gate memory cells arranged in rows and columns with word lines coupled to rows of floating-gate memory cells and bit lines coupled to columns of floating-gate memory cells, and wherein at least one of the floating-gate memory cells comprises:

a gate stack having a control-gate layer coupled to a word line and having a floating-gate layer interposed between the control-gate layer and a p-well;

an n^+-type drain region in the p-well coupled to a bit line;

an n^+-type source region in the p-well;

a source-line contact extending below the n^+-type source region to an n-well underlying the p-well; and

a conductive trace in the p-well and coupled between the n^+-type source region and the source-line contact.